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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Amador, et al.
Serial No.: 09/817,694
Filed: 03/26/2001
For: Fixture and Method for Uniform Electroless Metal Deposition on Integrated Circuit Bond Pads

Conf. No.: 9346
Docket No.: TI-30592
Examiner: Toledo, F. L.
Art Unit: 2823

Appeal Brief

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on October 14, 2003.

Elizabeth Austin

Dear Sir:

Pursuant to the Notice of Appeal mailed 08/12/03, Appellant submits this appeal brief in triplicate. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to deposit account number 20-0668 of Texas Instruments Incorporated.

Real Party in Interest

The real party in interest is Texas Instruments Incorporated.

Related Appeals and Interferences

No related appeals or interferences are known to Appellant.

Status of Claims

Claims 1-5 and 12-21 are pending in this application. Claims 13-15 and 18-21 have been withdrawn from consideration. Claims 1-5, 12, 16, and 17 are the subject of this appeal.

Claims 1-5, 12, 16, and 17 stand rejected under 35 U.S.C. 102(b) as being anticipated by Shacham-Diamand, et al. (U.S. Patent No. 5,830,805).

Status of Amendments

All amendments have been entered.

Summary of Invention

One embodiment of the invention is a method for controlled electroless plating of uniform metal layers onto exposed metallizations in integrated circuits positioned on the active surface of semiconductor wafers. The embodiment method includes the steps of: maintaining a plurality of wafers 101 approximately parallel to each other at predetermined distances 102 by supporting an edge of each wafer between a plurality of support means 104,105 (see page 9, first paragraph of the disclosure); immersing the wafers into an electroless plating solution 302 flowing in laminar motion at constant speed substantially parallel to the active surface of the wafers; rotating each of the wafers at constant speed and synchronously with each other by turning each of the plurality of support means (see page 9, second paragraph of the disclosure); and creating periodic relative motion in changing directions between the plating solution and the wafers, thereby uniformly plating layers onto the exposed metallizations by controlled electroless deposition (see page 11, first paragraph of the disclosure).

Issues

1. Whether Claims 1-5, 12, 16, and 17 are patentable under 35 U.S.C. 102(b) over Shacham-Diamand.

Grouping of Claims

Claims 1-5, 12, 16, and 17 stand or fall together.

Argument

1. Claims 1-5, 12, 16, and 17 are patentable under 35 U.S.C. 102(b) over Shacham-Diamand.

Claim 1 includes the steps of "maintaining a plurality of said wafers approximately parallel to each other at predetermined distances by supporting an edge of each said wafer between a plurality of support means" and "rotating each of said wafers at constant speed and synchronously with each other by turning each of said plurality of support means." Shacham-Diamand does not teach or suggest such steps. For example, in Figure 5, Shacham-Diamand shows wafers 220 held in holder 226. Figure 5 does not include sufficient detail to show how the edges of the wafers 220 are supported. No other possible support means are shown in Figure 5 other than holder 226. Holder 226 appears to be a unified structure and is thus not "a plurality of support means." Note also that since Shacham-Diamand does not teach a plurality of support means, rotation of the wafers is not performed by "turning each of said plurality of support means" as required by Claim 1. Appellant therefore submits that Claim 1 is patentable over Shacham-Diamand since that reference does not disclose all of the claimed features. Claims 2-5 depend from Claim 1 and are therefore patentable over Shacham-Diamand at least by virtue of their dependence from Claim 1.

Claim 2 includes the limitation wherein the "exposed metallizations are non-oxidized copper metallizations of bond pads positioned in said integrated circuits having copper metallizations." The Examiner refers to column 5 of Shacham-Diamand for support of the rejection. However, column 5 of Shacham-Diamand is concerned with the deposition of copper on a barrier layer such as

Ta or TiN. Shacham-Diamand thus does not concern plating on non-oxidized copper metallizations.

The Examiner has not provided an explanation of the basis of the rejection of Claims 12 and 16, but Claim 12 includes the steps of "supporting said wafer with a plurality of support means" and "rotating said wafer by rotating each of said plurality of support means." As argued above with respect to Claim 1, Shacham-Diamand does not teach or suggest such steps. Claims 16 and 17 depend from Claim 12 and are therefore patentable over Shacham-Diamand at least by virtue of their dependence from Claim 12.

Conclusion

In view of the above, Appellant appeals for the reversal of the rejections and allowance of Claims 1-5, 12, 16, and 17.

Respectfully submitted,

Michael K. Skrehot
Reg. No. 36,682

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APPENDIX

Claims on Appeal

1. A method for controlled electroless plating of uniform metal layers onto exposed metallizations in integrated circuits positioned on the active surface of semiconductor wafers, comprising the steps of:

maintaining a plurality of said wafers approximately parallel to each other at predetermined distances by supporting an edge of each said wafer between a plurality of support means;

immersing said wafers into an electroless plating solution flowing in laminar motion at constant speed substantially parallel to said active surface of said wafers;

rotating each of said wafers at constant speed and synchronously with each other by turning each of said plurality of support means; and

creating periodic relative motion in changing directions between said plating solution and said wafers, thereby uniformly plating layers onto said exposed metallizations by controlled electroless deposition.

2. The method according to Claim 1 wherein said exposed metallizations are non-oxidized copper metallizations of bond pads positioned in said integrated circuits having copper metallizations.

3. The method according to Claim 1 wherein said plurality of said wafers comprises between 10 and 30 wafers.

4. The method according to Claim 1 wherein said relative motion comprises a periodic superposition of directions and speeds of the motion of said wafers and the motion of said solution, thus creating periodically changing wafer portions where the directions and speeds are additive and where the directions and speeds are opposed and subtractive.

5. The method according to Claim 1 further comprising the steps of:

inserting the wafers into a clean-up or presoak bath;

removing the wafers from the clean-up or presoak bath; and

inserting the wafers into the plating solution.

12. A method of electroless plating of features on a semiconductor wafer, comprising the steps of:

supporting said wafer with a plurality of support means;

rotating said wafer by rotating each of said plurality of support means; and flowing plating solution over the surface of said wafer.

16. The method of Claim 12, further comprising the step of immersing said wafer and said support means in said plating solution.

17. The method of Claim 16, wherein said step of immersing said wafer comprises immersing said wafer and said support means in a tank and said step of flowing plating solution comprises flowing said solution from the bottom of said tank to the top of said tank.

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Status of Amendments

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Summary of Invention

One embodiment of the invention is a method for controlled electroless plating of uniform metal layers onto exposed metallizations in integrated circuits positioned on the active surface of semiconductor wafers. The embodiment method includes the steps of: maintaining a plurality of wafers 101 approximately parallel to each other at predetermined distances 102 by supporting an edge of each wafer between a plurality of support means 104,105 (see page 9, first paragraph of the disclosure); immersing the wafers into an electroless plating solution 302 flowing in laminar motion at constant speed substantially parallel to the active surface of the wafers; rotating each of the wafers at constant speed and synchronously with each other by turning each of the plurality of support means (see page 9, second paragraph of the disclosure); and creating periodic relative motion in changing directions between the plating solution and the wafers, thereby uniformly plating layers onto the exposed metallizations by controlled electroless deposition (see page 11, first paragraph of the disclosure).

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immersing said wafers into an electroless plating solution flowing in laminar motion at constant speed substantially parallel to said active surface of said wafers;

rotating each of said wafers at constant speed and synchronously with each other by turning each of said plurality of support means; and

creating periodic relative motion in changing directions between said plating solution and said wafers, thereby uniformly plating layers onto said exposed metallizations by controlled electroless deposition.

2. The method according to Claim 1 wherein said exposed metallizations are non-oxidized copper metallizations of bond pads positioned in said integrated circuits having copper metallizations.

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16. The method of Claim 12, further comprising the step of immersing said wafer and said support means in said plating solution.

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